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PATENT APPLICATION

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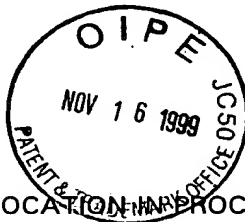
IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Robert Schreiber

Serial No.: 09/378,431

Filing Date: August 20, 1999

Title: FUNCTION UNIT ALLOCATION IN A PROCESSOR DESIGN



Examiner:

Group Art Unit:

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ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

- ☒ under 37 CFR 1.97(b), or
(Within three months of filing national application; or date of entry of international application; or before mailing date of first office action on the merits; whichever occurs last)
- ☐ under 37 CFR 1.97 (c) together with either a:
☐ Statement under 37 CFR 1.97(e), or
☐ a \$240.00 fee under 37 CFR 1.17(p), or
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs
- ☐ under 37 CFR 1.97 (d) together with a:
☐ Statement under 37 CFR 1.97(e), and
☐ a petition under 37 CFR 1.97(d)(2), and
☐ a \$130.00 petition fee set forth in 37 CFR 1.17(i).
(Filed after final action or notice of allowance, whichever occurs first, but before payment of the issue

Please charge to Deposit Account **08-2025** the sum of \$0.00. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **08-2025** pursuant to 37 CFR 1.25.

☒ Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Citation together with copies, of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

☐ A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individuals(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231.

Date of Deposit: 11/11/99

Typed Name: Mark L. Becker, Esq.

Signature: 

Respectfully submitted,

Robert Schreiber

By 

Mark L. Becker, Esq.

Attorney/Agent for Applicant(s)

Reg. No. 31,325

Date:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re application of

Robert S. Schreiber

Serial No.: 09/378,431

Filed: August 20, 1999

For: FUNCTION UNIT ALLOCATION IN
PROCESSOR DESIGN



CERTIFICATE OF MAILING

I HEREBY CERTIFY THAT THIS PAPER AND THE DOCUMENTS REFERRED TO AS BEING ATTACHED OR ENCLOSED HERewith ARE BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE ON November 11, 1999, AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO: ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, DC 20231.

Mark L. Becker
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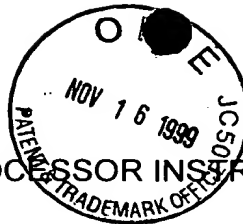
INFORMATION DISCLOSURE STATEMENT

ASSISTANT COMMISSIONER FOR PATENTS
Washington, DC 20231

Applicants submit herewith information of which they are aware, and which they believe may be material to the examination of the application and in respect of which there may be a duty to disclose in accordance with 37 C.F.R. § 1.56. The information is listed on the attached Form PTO-1449 and copies are enclosed.

Applicant calls the Examiner's attention to the following co-pending U.S. patent applications:

- 1) Application No. 09/378,395
For: AUTOMATIC DESIGN OF VLIW PROCESSORS
Applicants: Gupta et al.
- 2) Application No. 09/378,596
For AUTOMATIC DESIGN OF PROCESSOR DATABASE
Applicants: Gupta et al.
- 3) Application No. 09/378,601
For: PROGRAMMATIC SYNTHESIS OF A MACHINE DESCRIPTION FOR RETARGETING A COMPILER
Applicants: Gupta
- 4) Application No. 09/378,293
For AUTOMATIC DESIGN OF VLIW INSTRUCTION FORMATS
Applicants: Gupta et al.



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- 5) Application No. 09/378,394
For: AUTOMATED DESIGN OF PROCESSOR INSTRUCTION UNITS
Applicants: Gupta et al.
- 6) Application No. 09/378,295
For INTERCONNECT MINIMIZATION IN PROCESSOR DESIGN
Applicants: Robert S. Schreiber
- 7) Application No. 09/378,298
For: PROGRAMMATIC SYNTHESIS OF PROCESSOR ELEMENT ARRAYS
Applicants: Robert S. Schreiber et al.
- 8) Application No. 09/378,290
For AUTOMATED DESIGN OF PROCESSOR SYSTEMS USING FEEDBACK
FROM INTERNAL MEASUREMENTS OF CANDIDATES SYSTEMS
Applicants: Schlansker et al.
- 9) Application No. 09/378,393
For: PROGRAMMATIC ITERATION SCHEDULING FOR PARALLEL
PROCESSORS
Applicants: Robert S. Schreiber et al.
- 10) Application No. 09/378,397
For PROGRAMMATIC METHOD FOR REDUCING COST OF CONTROL IN
PARALLEL PROCESSORS
Applicants: Alain Darté et al.

No fee is required since this document is being submitted within 3 months of the filing date.

Respectfully submitted,

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LEIGH & WHINSTON, LLP

By

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Date: November 11, 1999

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